WHAT IS CLAIMED IS:

1.   A testing method for a semiconductor device, having wirings composed of copper or an alloy mainly composed of copper, comprising:

executing an acceleration test for eliminating an initial failure of the wirings due to stress migration; and

checking whether or not the wirings are broken.

2.   The testing method as in claim 1, wherein executing the acceleration test comprises holding a temperature of the semiconductor device in a first temperature zone covering ±40°C of a temperature at which the stress migration is most accelerated.

3.   The testing method as in claim 2, wherein the temperature at which the stress migration is most accelerated is a test temperature when an acceleration factor AF is maximized, the acceleration factor AF is obtained based on a time to failure at a maximum temperature in actual use of the semiconductor device and a time to failure at the test temperature of the semiconductor device.

4.   The testing method as in claim 3, wherein the acceleration factor AF has a relationship shown by following Expression

$$AF = \{C(TO - Ta)^{-n} \cdot exp(Ea/kTa)\}/\{C(TO - Tatest)^{-n} \cdot exp(Ea/kTatest)\}$$

where, Ta is the maximum temperature, Tatest is the test temperature, C and n are constants inherent to the semiconductor device, TO

is a stress free temperature, Ea is activation energy of growth

of voids in the wirings, and k is the Boltzmann constant.

5.   The testing method as in claim 2, wherein executing the

acceleration test comprises holding the temperature of the

5   semiconductor device in the first temperature zone for at least

0.4 hour.

6.   ' The testing method as in claim 2, wherein executing the

acceleration test comprises holding the temperature of the

semiconductor device in the first temperature zone from 0.4 hour

10   to two hours.

7.   The testing method as in claim 2, wherein executing the

acceleration test comprises increasing and decreasing the

temperature of the semiconductor device at least once in a second

temperature zone covering ±40°C of a reference temperature set

15   in the first temperature zone covering ±40°C of a temperature

at which the stress migration is most accelerated.

8.   The testing method as in claim 7, wherein executing the

acceleration test comprises increasing and decreasing the

temperature of the semiconductor device in the second temperature

20   zone for at least 0.4 hour.

9.   The testing method as in claim 7, wherein executing the

acceleration test comprises increasing and decreasing the

temperature of the semiconductor device in the second temperature

zone from 0.4 hour to two hours.

25   10.   The testing method as in claim 1, wherein after semiconductor

elements composing the semiconductor device are formed on a

semiconductor substrate, executing the acceleration test when the wirings are formed in wiring layers through interlayer insulation films and the semiconductor elements are connected to each other via the wirings.

5   11.   A manufacturing method for a semiconductor device comprising:

forming semiconductor elements configured to implement the semiconductor device on a semiconductor substrate; and

forming wirings composed of copper or an alloy mainly
10   composed of copper in wiring layers through interlayer insulation films to connect the semiconductor elements to each other,

wherein the forming of the wirings comprises holding a temperature of the wirings in a first temperature zone covering ±40°C of a temperature at which a stress migration is most
15   accelerated.

12.   The testing method as in claim 11, wherein the temperature at which the stress migration is most accelerated is a test temperature when an acceleration factor AF is maximized, the acceleration factor AF is obtained based on a time to failure
20   at a maximum temperature in actual use of the semiconductor device and a time to failure at the test temperature of the semiconductor device.

13.   The testing method as in claim 12, wherein the acceleration factor AF has a relationship shown by following Expression
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$$AF = \{C(TO - Ta)^{-n} \cdot \exp(Ea/kTa)\}/\{C(TO - Tatest)^{-n} \cdot \exp(Ea/kTatest)\}$$

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where, Ta is the maximum temperature, Tatest is the test temperature,

C and n are constants inherent to the semiconductor device, TO

is a stress free temperature, Ea is activation energy of growth

of voids in the wirings, and k is the Boltzmann constant.

14.   The manufacturing method as in claim 11, wherein the forming

of the wirings comprises:

depositing the interlayer insulation films over the

semiconductor substrate;

forming contact holes and wiring trenches in the interlayer

insulation films;

depositing metal films composed of copper or an alloy mainly

composed of copper on the interlayer insulation films;

holding the temperature of the metal films in the first

temperature zone; and

forming the wirings buried in the contact holes and the

wiring trenches by removing a part of the metal films.

15.   The manufacturing method as in claim 11, wherein the forming

of the wirings comprises:

depositing the interlayer insulation films over the

semiconductor substrate;

forming contact holes and wiring trenches in the interlayer

insulation films;

depositing metal films composed of copper or an alloy mainly

composed of copper on the interlayer insulation films;

forming the wirings buried in the contact holes and the

wiring trenches by removing a part of the metal films; and

maintaining the temperature of the wirings within the first

temperature zone.

16. A manufacturing method for a semiconductor device

5 comprising:

forming semiconductor elements configured to implement the

semiconductor device on a semiconductor substrate; and

forming wirings composed of copper or an alloy mainly

composed of copper in wiring layers through interlayer insulation

10 films to connect the semiconductor elements to each other,

wherein the forming of the wirings comprises increasing

and decreasing the temperature of the semiconductor device in

a second temperature zone covering ±40°C of a reference temperature

set in a first temperature zone covering ±40°C of a temperature

15 at which the stress migration is most accelerated.

17. The testing method as in claim 16, wherein the temperature

at which the stress migration is most accelerated is a test

temperature when an acceleration factor AF is maximized, the

acceleration factor AF is obtained based on a time to failure

20 at a maximum temperature in actual use of the semiconductor device

and a time to failure at the test temperature of the semiconductor

device.

18. The testing method as in claim 17, wherein the acceleration

factor AF has a relationship shown by following Expression

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$$AF = \{C(TO - Ta)^{-n} \cdot \exp(Ea/kTa)\}/\{C(TO - Tatest)^{-n} \cdot \exp(Ea/kTatest)\}$$

where, Ta is the maximum temperature, Tatest is the test temperature, C and n are constants inherent to the semiconductor device, TO is a stress free temperature, Ea is activation energy of growth

5   of voids in the wirings, and k is the Boltzmann constant.

19.   The manufacturing method as in claim 16, wherein the forming of the wirings comprises:

depositing the interlayer insulation films over the semiconductor substrate;

10   forming contact holes and wiring trenches in the interlayer insulation films;

depositing metal films composed of copper or an alloy mainly composed of copper on the interlayer insulation films;

increasing and decreasing the temperature of the metal films

15   in the second temperature zone; and

forming the wirings buried in the contact holes and the wiring trenches by removing a part of the metal films.

20.   The manufacturing method as in claim 16, wherein the forming of the wirings comprises:

20   depositing the interlayer insulation films over the semiconductor substrate;

forming contact holes and wiring trenches in the interlayer insulation films;

depositing metal films composed of copper or an alloy mainly

25   composed of copper on the interlayer insulation films; and

forming the wirings buried in the contact holes and the

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wiring trenches by removing a part of the metal films; and

increasing and decreasing the temperature in the second

temperature zone.